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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,554	01/12/2004	Yuichi Toriumi	118301	9278

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EXAMINER	
LUI, DONNA V.	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,554	TORIUMI ET AL.	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-6,9-15,and 18-20* is/are rejected.

7)☒ Claim(s) *7,8,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/23/2005; 5/06/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Inventorship

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections

3. Claims 1, 19, and 20 are objected to because of the following informalities: grammatical errors. Appropriate correction is required. The following is a suggestion for correction.

Claim 1, line 5: distributed from two opposite sides toward an inside of the electro-optical device in a shape

Claim 19, line 4: from two opposite sides toward an inside of the electro-optical device in a shape of comb

Claim 20, line 4: distributed from the first and second sides toward an inside of the electro-optical device in a

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-6, 9-15, and 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miwa Yuichi (English translation of JP 2001-051656) in view of Tajima et al. (Pub. No.: US 2003/0030614 A1) and further in view of Kanbara (Patent No.: US 6,621,481 B1).

With respect to **Claim 1**, Yuichi teaches a display driver *(See Drawing 3, element 56)* which drives a plurality of data lines *(element Ld)* of an electro-optical device *([0001])* which includes a plurality of scan lines *([0025], scan lines ~ to gate lines)*, the data lines, and a switching element *([0024], lines 4-8; p-SiTFT ~ switching element)* connected with one of the scan lines and one of the data lines.

Yuichi teaches a pixel electrode is inherently connected with the switching element because in order for a pixel electrode to emit light the voltage applied to the switching element through the scan line allows the data line to supply the appropriate gray-scale voltage.

Yuichi teaches the data lines including data line groups alternately distributed from two opposite sides toward an inside of the electro-optical device in a shape of comb teeth *(See*

Drawing 3), each of the data line groups *(See Drawing 3, data line groups: A, B, C, D, ... O, P)* consisting of a predetermined number of the data lines *(Yuichi: [0031], lines 1-5)*, and the display driver comprising: a first shift register *(See Drawing 4 and 12, shift register 1; [0059], section corresponding to odd data lines; note that attention is directed to figure 12 to show that the driving is broken up into blocks and thus there is more than one shift register)* shifts a first shift start signal *([0033], lines 1-3; a first shift start signal is equivalent to a sampling pulse)* in a first shift direction *([0059]; a first shift direction is equivalent to an ascending order)* and outputs shift output *([0055], line 2)* and a second shift register *(See Drawing 4 and 12, shift register 1; [0059], section corresponding to even data lines)*, shifts a second shift start signal *([0033], lines 1-3; a secondt shift start signal is equivalent to a sampling pulse)* in a second shift direction *([0059]; a second shift direction is equivalent to an descending order)* opposite to the first shift direction based on the first shift clock on the second clock line, and outputs shift output *([0055], line 2)*.

Yuichi teaches the display driver to further comprise: a first data latch *(See Drawing 4 and 12; [0033], lines 3-5; note that attention is directed to figure 12 to show that the driving is broken up into blocks and thus there is more than one data latch) ([0059]; note that the first data latch relates to data is outputted in ascending order)* which holds the gray-scale data corresponding to one of the data lines based on the shift output of the first shift register, a second data latch *(See Drawing 4 and 12; [0033], lines 3-5; note that attention is directed to figure 12 to show that the driving is broken up into blocks and thus there is more than one data latch) ([0059]; note that the second data latch relates to data is outputted in descending order)* which holds the gray-scale data corresponding to one of the data lines based on the shift output of the

second shift register, a data line driver circuit *(See Drawing 4, element 56; [0039], line 5)* including a plurality of output sections *(element 7: output sections)*, each of the data output sections driving one of the data lines based on the gray-scale data held in the first or second data latch and being disposed corresponding to the arrangement order of the data lines *([0044], lines 1-5)*.

Yuichi does not mention a gray-scale bus to which gray-scale data is supplied corresponding to an arrangement order of each of the data lines.

Yuichi does not mention that the first and second shift register includes a plurality of flip-flops and does not mention the shifting of the signal is based on a first shift clock.

Yuichi does not mention the first or second data latch includes a plurality of flip-flops.

Yuichi does not mention first and second clock lines to which a first or second shift clock is supplied.

Yuichi does not mention a clock switch circuit which outputs one of the first and second shift clocks to the first clock line and outputs the other of the first and second shift clocks to the second clock line based on a mode setting signal.

Tajima teaches a gray-scale bus to which gray-scale data is supplied corresponding to an arrangement order of each of the data lines *(See figure 12; [0008])*. Tajima teaches a shift register includes a plurality of flip-flops and that the shifting of the signal is based on a shift clock *(See figure 6, element 61: shift register; [0010], lines 1-5; [0072], lines 10-18)*. Tajima teaches a data latch *(See figure 1, element 3A; figure 4: data output controlling circuit of element 3A; figure 5, element 63; note that the data latch is comprised of figure 4 and element 63)* which includes a plurality of flip-flops *([0070]; L1, L2, ... Ln: flip-flops)*, each of which holds gray-

scale data corresponding to one of the data lines based on the shift output of the shift register *(See figures 4 and 6).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a gray-scale bus to which gray-scale data is supplied corresponding to an arrangement order of each of the data lines, a shift register including a plurality of flip-flops such that the shifting of the signal is based on a shift clock and a data latch which includes a plurality of flip-flops, as taught by Tajima, to the display driver of Yuichi, so as to lower power consumption, and reduce electromagnetic interference occurring when gray-scale data is transferred in a bus wiring of a display panel *(Tajima: [0049], lines 11-14).*

Kanbara teaches a display device *(See figure 1)* where a first and second clock line to which a first and second shift clock is supplied *(See figure 4, CLK: first shift clock and inverted CLK: second shift clock are supplied to two separate clock lines; column 9, lines 40-44).* Kanbara teaches a clock switch circuit *(DCNT; column 9, lines 40-44; column 19, lines 16-22)* which outputs one of the first and second shift clocks to the first clock line and outputs the other of the first and second shift clocks to the second clock line based on a mode setting signal *(column 19, lines 26-34 and lines 45-54; note that the mode setting signal for one mode are signals Φ3 and Φ4 for a forward-direction operation and another mode setting signal are signals Φ1 and Φ2 for a reverse-direction operation).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have first and second clock lines to which a first or second shift clock is supplied and to have a clock switch circuit which outputs one of the first and second shift clocks to the first clock line and outputs the other of the first and second shift clocks to the second clock

line based on a mode setting signal, as taught by Kanbara, to the display driver of Yuichi, as modified by Tajima, so as to provide a device capable of arbitrarily changing the direction of an image to be displayed by simple control *(column 1, line 66 to column 2, line 1).*

With respect to **Claim 2**, the display driver of Yuichi, as modified by Tajima and Kanbara in claim 1, teaches the data line driver circuit *(Yuichi: Drawing 3, element 56)* drives the data lines *(Yuichi: Drawing 3, Ld)* from a first side *(Yuichi: Drawing 3 and 4, data lines (1, 3, ..., 299); note that the first side is equivalent to an upper section)* of the electro-optical device based on data held in the flip-flops of the first data latch, and drives the data lines from a second side *(Yuichi: Drawing 3 and 4, data lines (2, 4, ..., 300); note that the second side is equivalent to a lower section)* of the electro-optical device which faces the first side based on data held in the flip-flops of the second data latch.

With respect to **Claims 3 and 4**, the display driver as defined in claims 1 and 2 respectively, Kanbara teaches the clock switch circuit *(DCNT; column 9, lines 40-44; column 19, lines 16-22)* outputs a first reference shift clock to the first clock line as the first shift clock *(See figure 4, CLK: first shift clock; column 9, lines 40-44; note that the first reference shift clock is the same as the first shift clock)* and outputs a second reference shift clock *(See figure 4, inverted CLK: second shift clock; column 9, lines 40-44; note that the second reference shift clock is the same as the second shift clock)* to the second clock line as the second shift clock when the mode setting signal is at a first level *(column 19, lines 26-34 and lines 45-54; note that the mode setting signal at a first level is equivalent to the signals Φ3 and Φ4 at a low level for a forward-*

direction operation), and outputs the second reference shift clock to the first clock line as the first shift clock and outputs the first reference shift clock to the second clock line as the second shift clock when the mode setting signal is at a second level *(note that the mode setting signal at a second level is equivalent to the signals Φ1 and Φ2 at a low level for a reverse-direction operation)*.

With respect to **Claims 5 and 6**, the display driver as defined in claims 3 and 4 respectively, Kanbara teaches a shift clock generation circuit which generates the first and second reference shift clocks based on a reference clock *(See figure 4; DCNT; column 9, lines 40-44; the reference clock is the signal CLK, where DCNT generates the first reference shift clock to be the same as the reference clock and the second reference shift clock is the inversion of the reference clock)*, wherein a shift operation period by each of the first and second shift registers includes a period in which phases of the first and second reference shift clocks are reversed *(See figures 9 and 10)*.

With respect to **Claim 9**, the display driver as defined in claim 2, Yuichi teaches a direction from the first side to the second side in which the data lines extend is the same as the first or second shift direction *(See Drawing 3; note that the each data line extends from the upper section to the lower section or vice versa is along the same direction as the ascending or descending shift direction of the output data from the data driver 56)*.

With respect to **Claims 10-15 and 18**, the display driver as defined in claims 1, 2, 3, 4, 5, 6, and 9, Yuichi teaches the scan lines extend along a long side of the electro-optical device *([0025], lines 1-6; note that the scan lines extend in a longitudinal direction along the long side of the device)* and the data lines extend along a short side of the electro-optical device, the display driver is disposed along the short side *(See Drawing 3, note that the longest side of the data driver 56, and each branch of the data lines extends in a latitude direction along the short side of the device)*.

With respect to **Claim 19**, claim 19 differs from claim 1 only in that claim 19 is an electro-optical device *(Yuichi: [0024], lines 1-4)* having the display driver of claim 1 and additionally recites the limitation "a scan driver which scans the scan lines". Yuichi inherently teaches a scan driver which scans the scan lines in order for the electro-optical device to function.

With respect to **Claim 20**, claim 20 differs from claim 19 only in that claim 20 recites the additional limitation "a display panel which has first and second sides facing each other" *(Yuichi: Drawing 3 and 4, data lines (1, 3, ..., 299): upper section, data lines (2, 4, ..., 300): lower section; note that the first side is equivalent to an upper section and the second side is equivalent to a lower section)*.

Allowable Subject Matter

5. **Claims 7-8 and 16-17** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to **Claims 7 and 8**, none of the prior art teaches the first and second shift start signals are signals having the same phase, nor does the prior art teach a shift generation circuit generates the second reference shift clock by dividing the frequency of the reference clock, and generates the first reference shift clock which has a pulse in a first-stage capture period for capturing the first shift start signal into the first shift register and has a phase which is a reverse of a phase of the second reference shift clock in a data capture period after the first-stage capture period has elapsed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
SUPERVISORY PATENT EXAMINER